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#### **ABSTRACT OF THE DISCLOSURE**

A multi-queue single-FIFO scheme for quality of service oriented communication. According to the invention, an arbiter maintains a number of next access pointers for multiple queues storing data packets to be transmitted. The  
5 arbiter also determines which queue is to be serviced next contingent upon a quality of service policy and then fetches at least one data packet, identified by the chosen queue's next access pointer, through a peripheral bus by means of  
10 direct memory access (DMA). A single FIFO buffer is connected to the arbiter to store and manage the fetched data packet in a first-in-first-out manner. Following the FIFO buffer, physical layer interface logic accepts each data packet, if available, and prepares the data packet for  
15 transmission on a physical medium.